



# PIMD3-Q

50 V, 100 mA NPN/PNP resistor-equipped transistor;  
R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$

1 August 2025

Product data sheet

## 1. General description

NPN/PNP Resistor-Equipped Transistors (RET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

## 4. Quick reference data

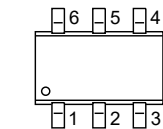
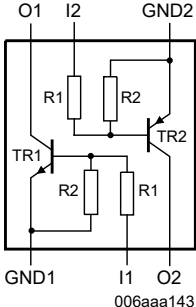
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
I <sub>O</sub>	output current		-	-	100	mA
R1	bias resistor 1 (input)		7	10	13	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	

50 V, 100 mA NPN/PNP resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p><b>TSOP6 (SOT457)</b></p>	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PIMD3-Q	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

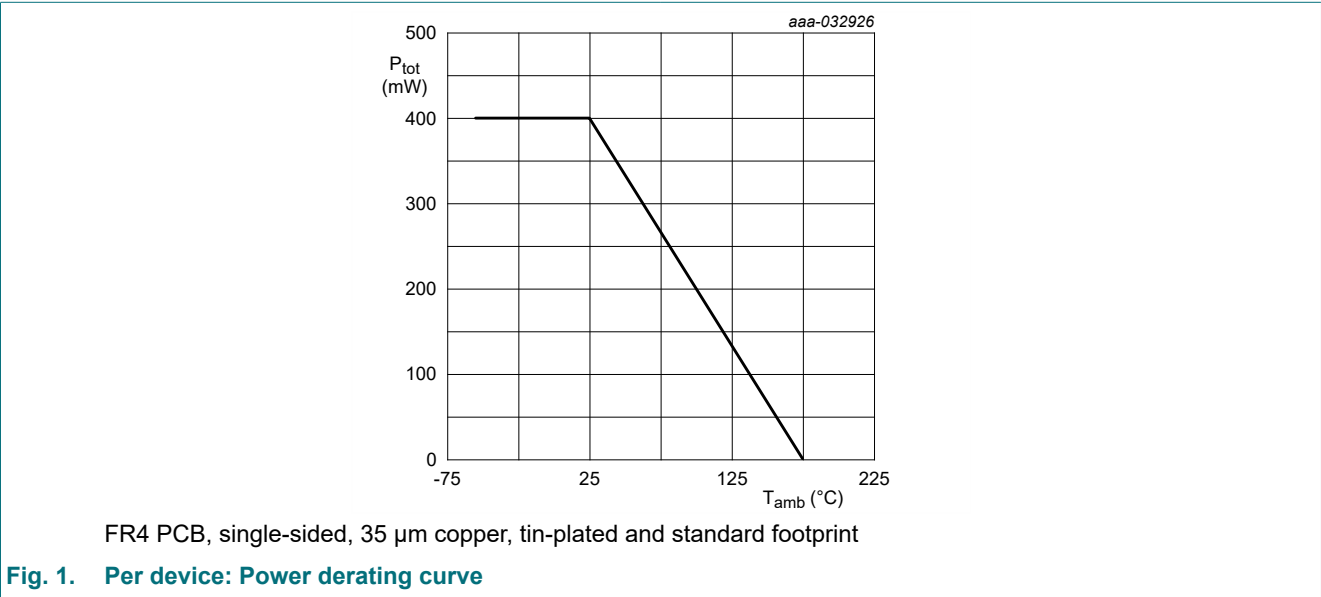
Type number	Marking code
PIMD3-Q	M7

8. Limiting values

Table 5. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	10	V
V <sub>I</sub>	input voltage	input voltage TR1		-	40	V
				-	-10	V
		input voltage TR2		-	10	V
				-	-40	V
I <sub>O</sub>	output current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	250	mW
Per device						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	400	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.

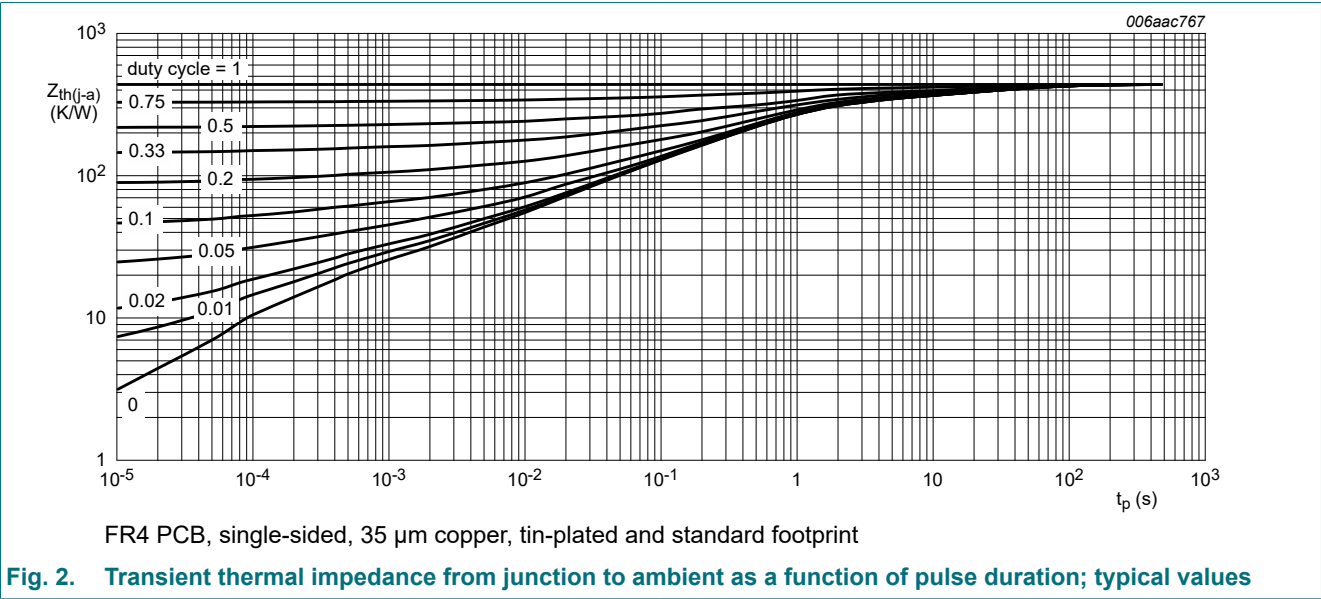


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	313	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\text{ }\mu\text{A}$ ; $I_E = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\text{ mA}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		50	-	-	V
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50\text{ V}$ ; $I_E = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	1	$\mu\text{A}$
		$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_j = 150\text{ }^{\circ}\text{C}$		-	-	5	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}$ ; $I_C = 0\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	400	$\mu\text{A}$
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}$ ; $I_C = 5\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		30	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}$ ; $I_B = 0.5\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$ ; $I_C = 100\text{ }\mu\text{A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$ ; $I_C = 10\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		2.5	1.8	-	V
R1	bias resistor 1 (input)			7	10	13	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
TR1 (NPN)							
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}$ ; $I_E = 0\text{ A}$ ; $i_e = 0\text{ A}$ ; $f = 1\text{ MHz}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	2.5	pF
$f_T$	transition frequency	$V_{CE} = 5\text{ V}$ ; $I_C = 10\text{ mA}$ ; $f = 100\text{ MHz}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	230	-	MHz
TR2 (PNP)							
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}$ ; $I_E = 0\text{ A}$ ; $i_e = 0\text{ A}$ ; $f = 1\text{ MHz}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	3	pF
$f_T$	transition frequency	$V_{CE} = -5\text{ V}$ ; $I_C = -10\text{ mA}$ ; $f = 100\text{ MHz}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	180	-	MHz

[1] Characteristics of built-in transistor

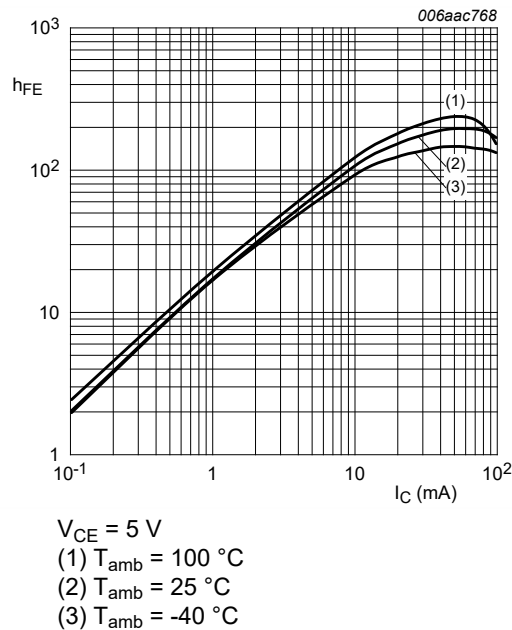


Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values

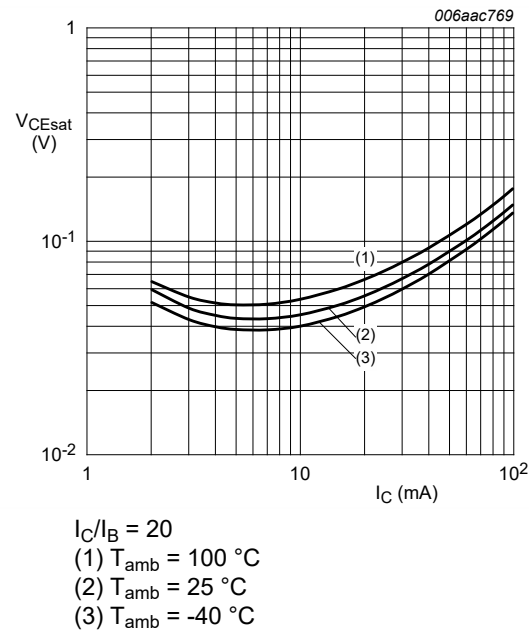


Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

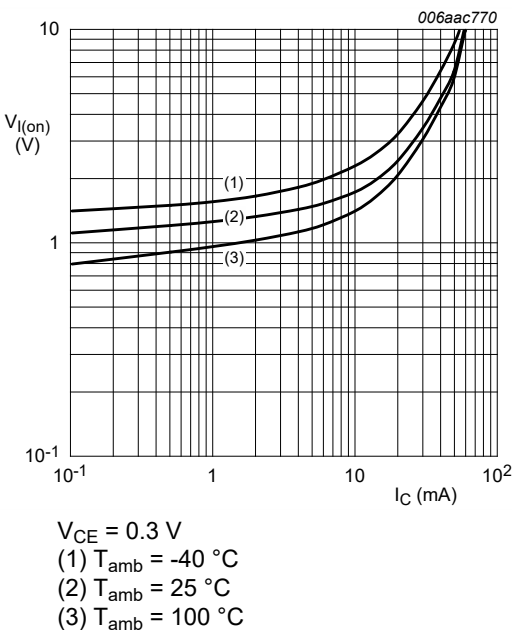


Fig. 5. TR1 (NPN): On-state input voltage as a function of collector current; typical values

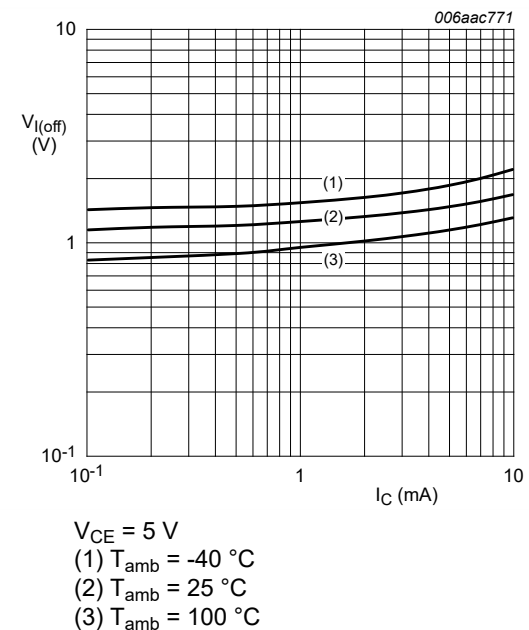


Fig. 6. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

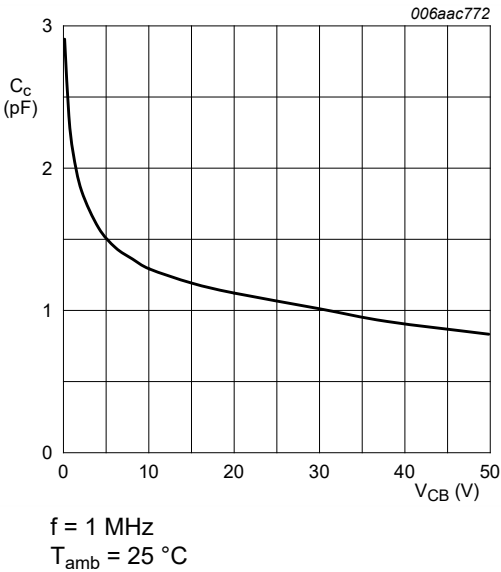


Fig. 7. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values

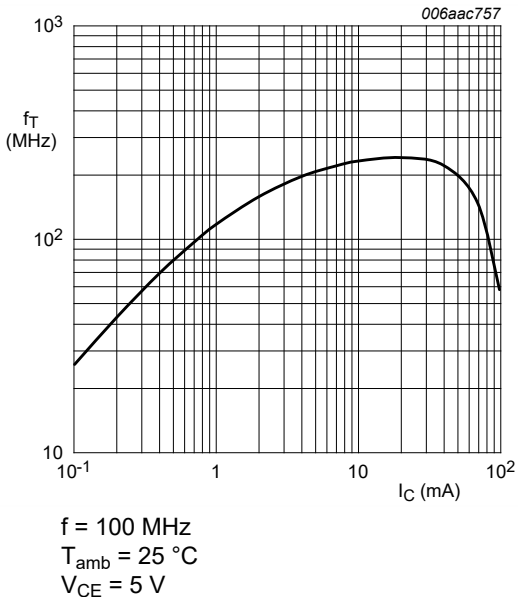


Fig. 8. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor

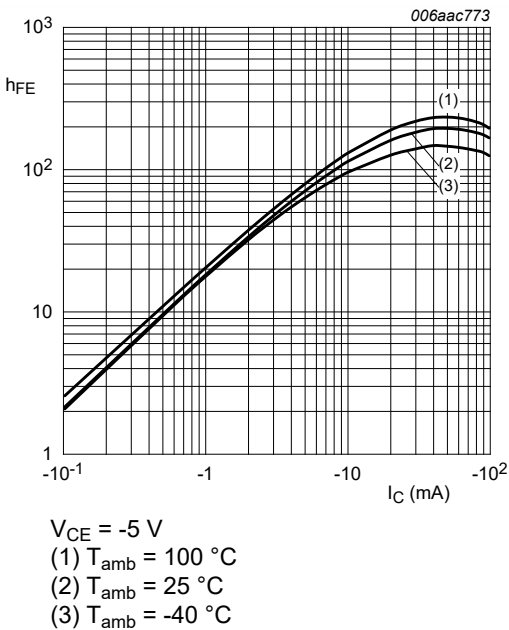


Fig. 9. TR2 (PNP): DC current gain as a function of collector current; typical values

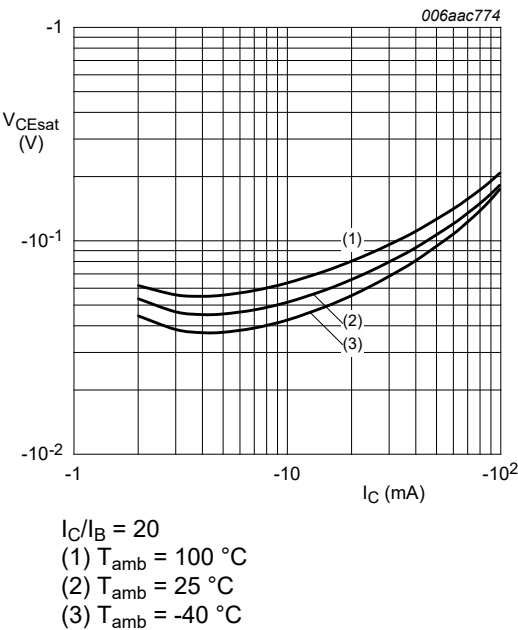


Fig. 10. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

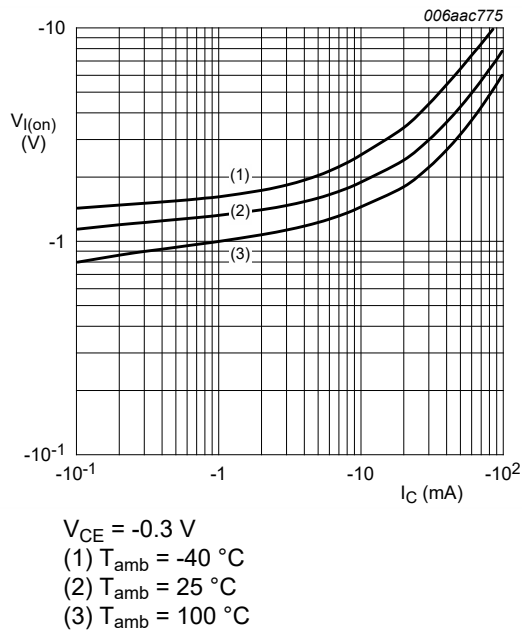


Fig. 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values

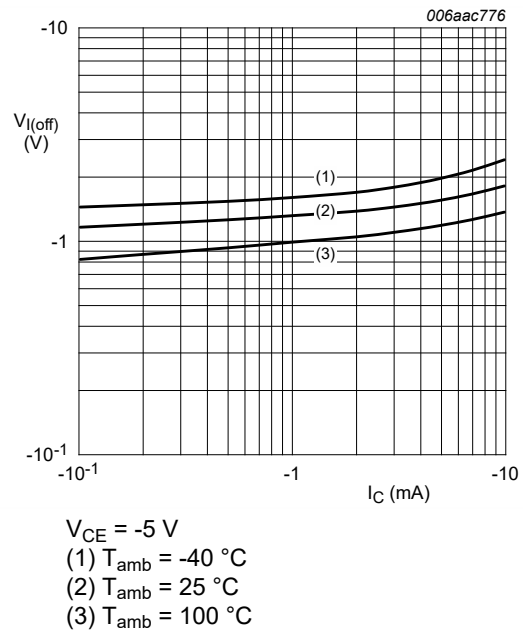


Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

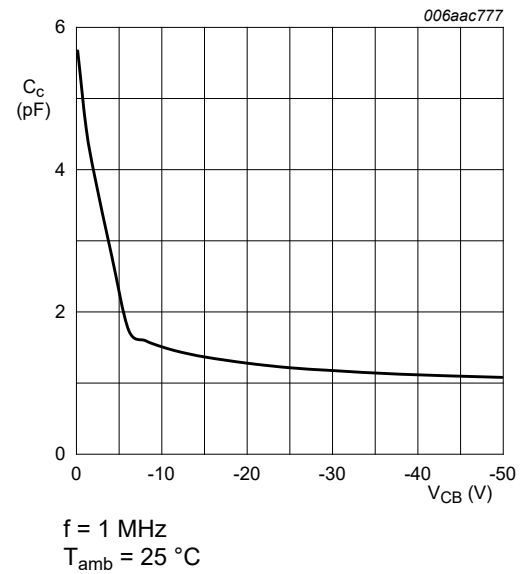


Fig. 13. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values

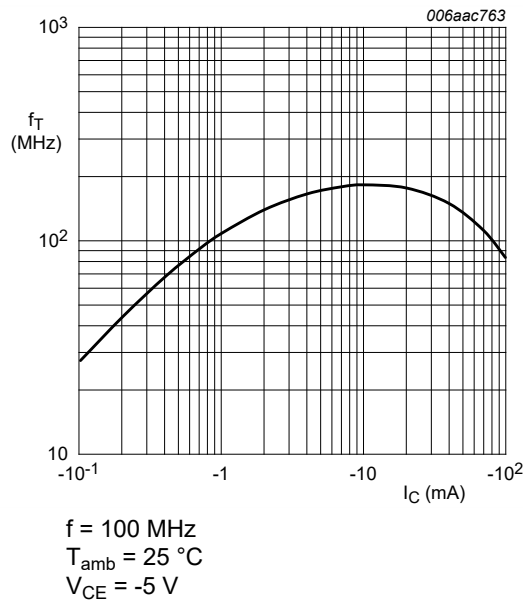


Fig. 14. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_4) - V(I_3)}{R1 \cdot (I_4 - I_3)} - 1$$

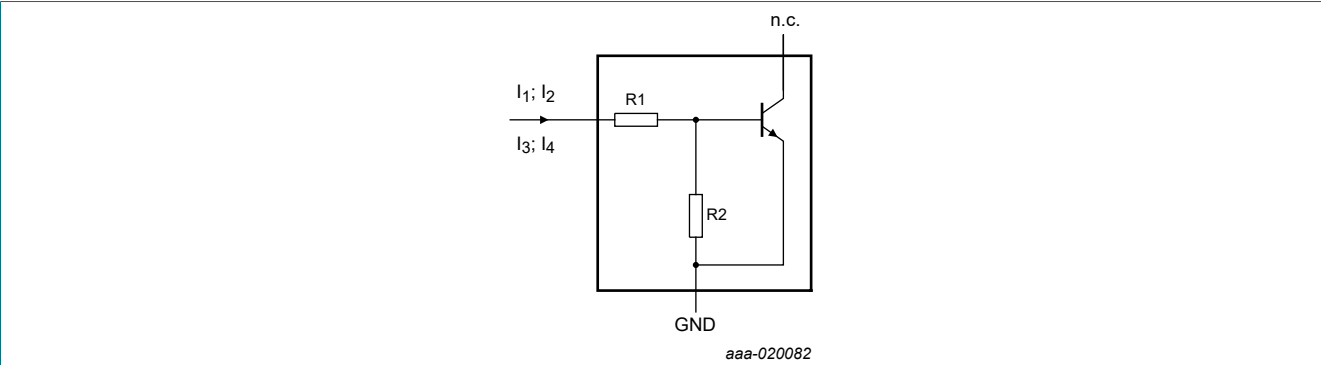


Fig. 15. NPN transistor: Resistor test circuit

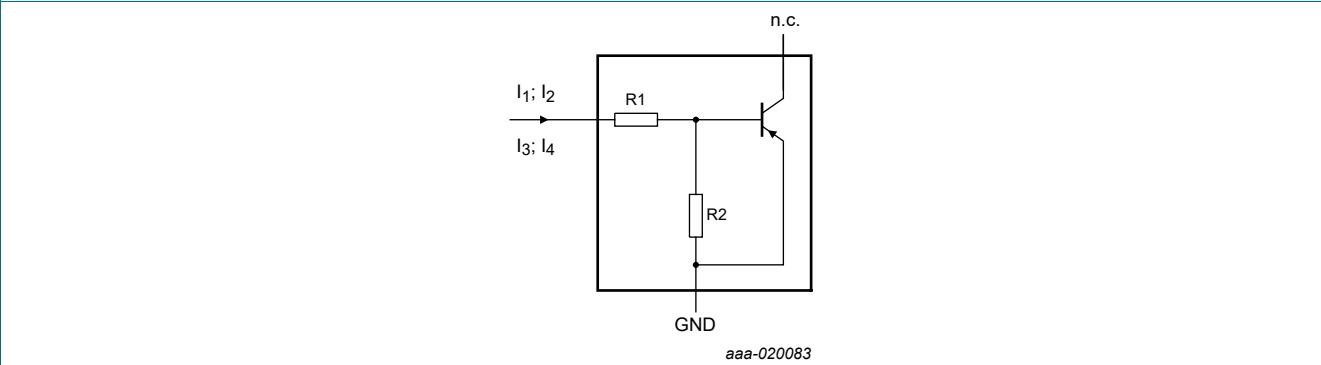


Fig. 16. PNP transistor: Resistor test circuit

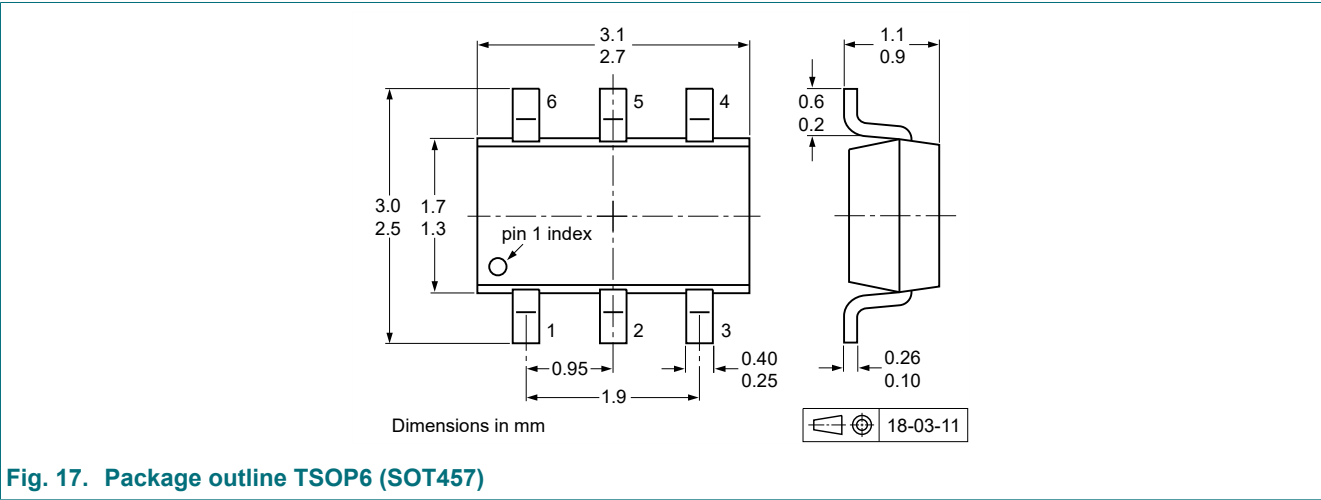
Resistor test conditions

Table 8. Resistor test conditions

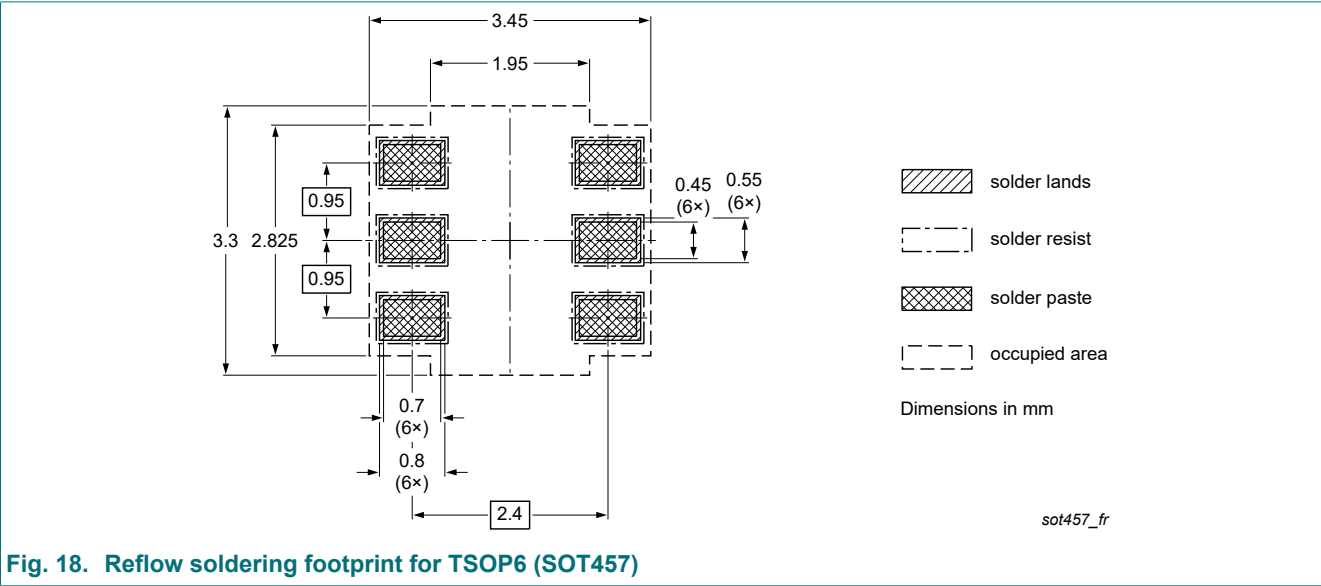
Per transistor; for the PNP transistor with negative polarity

Product	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>
PIMD3-Q	10	10	350 μA	450 μA	-350 μA	-450 μA

12. Package outline



13. Soldering



50 V, 100 mA NPN/PNP resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ

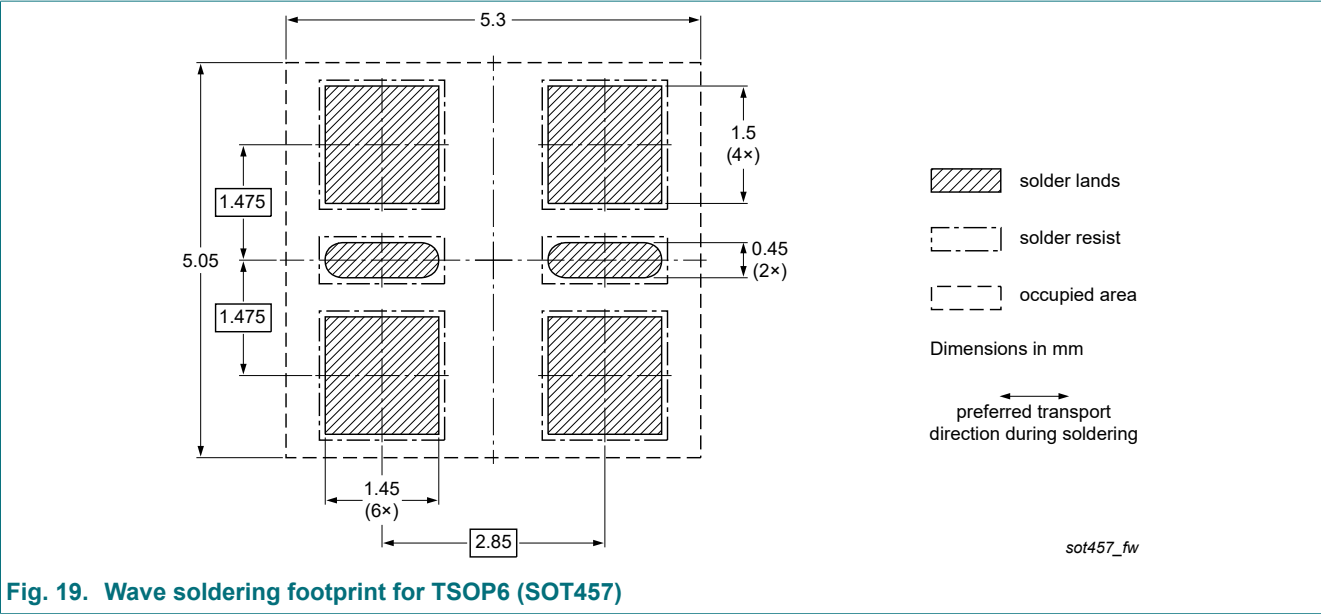


Fig. 19. Wave soldering footprint for TSOP6 (SOT457)

50 V, 100 mA NPN/PNP resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PIMD3-Q v.1	20250801	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 1 August 2025